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SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

CONFIGURATION FOR DIGITAL-ANALOG CONVERSION OF HIGH-FREQUENCY DIGITAL INPUT SIGNAL INTO CARRIER-FREQUENCY ANALOG OUTPUT SIGNAL

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and hereby claims priority to German Application No. 102 27 856.8 filed on 19 August 2002 and European Application No. 02018602.9 filed on 19 August 2002, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The invention relates to a configuration for the digital-analog conversion of a high-frequency digital input signal into a carrier-frequency analog output signal.

2. Description of the Related Art

[0003] Architectures for the generation of a broadband, carrier-frequency output signal are known in which, in a low frequency range, a digital input signal is converted into an analog signal using a digital-analog converter, and then reconverted into the carrier-frequency output signal using one or more mixing stages.

[0004] Furthermore, digital-analog converter architectures are known in which a carrier-frequency output signal is generated from a high-frequency digital input signal without further frequency conversion. The carrier-frequency analog output signal in this case also has unwanted carrier frequencies in addition to a desired carrier frequency. These unwanted carrier frequencies can be caused, for example, by a less than perfect digital input signal or by various unwanted modulation mechanisms.

[0005] In the described architectures, cost-intensive filters with high quality or mixers with high linearity, which are always configured on the output end and which must be adjusted to a required carrier frequency range in each case, are necessary. These must be replaced, at great expense, if a change in carrier frequency range is required.

SUMMARY OF THE INVENTION

[0006] An object of this invention is therefore to design a configuration for digital-analog conversion in such a way that it can be adjusted to various carrier frequency ranges without great cost.

[0007] A configuration for digital-analog conversion according to one aspect of the invention has an integrated filter characteristic, thus eliminating the need for cost-intensive mixers or filters at the output end. D/A converters are connected parallel to one another and specific coefficients are assigned to each of the individual D/A converters. This enables the configuration to be ideally adjusted to a required carrier frequency range.

[0008] A configuration according to the invention can be adjusted to different carrier frequency ranges by modifying the clock frequency of the D/A converters accordingly.

[0009] According to the invention, it is particularly preferable for a Finite Impulse Response (FIR) filter characteristic to be realized and/or integrated into the configuration through the selection of the coefficients that are specifically assigned to the D/A converters and of the delay times that are specifically assigned to the delay elements. The consecutive coefficients correspond to a sampling of an impulse response from a filter that has a required filter characteristic. In this way the carrier-frequency output signal has a higher spectral purity compared to a form implemented without filter characteristic.

[0010] The FIR filter characteristic integrated according to the invention is scalable using a clock frequency of a clock signal. This may be derived from or identical to the clock frequency of the A/D converters. Since the clock frequency usually varies in proportion to the carrier frequency, the filter characteristic is automatically adjusted in this invention.

[0011] If there is a change in the required carrier frequency range, the FIR filter characteristic is reset accordingly via the clock frequency. There is no replacement of hardware components.

[0012] If the accuracy and the number of the FIR filter coefficients correspond to the requirements of a new mobile radio standard, then it is possible to switch frequency range directly via the clock frequency, in which case software might be used to implement the switch.

[0013] A configuration according to the invention enables expenditure on filters to be considerably reduced, for any carrier frequency range, by prefiltering. Together with a

corresponding power output stage, the elimination of the need for frequency-specific filtering at the transmitter end makes for high quality.

[0014] In particular, quantization noise formed by ΣΔ converters on the input signal can easily be suppressed by using a configuration according to the invention.

[0015] The filter function of a configuration according to the invention can be influenced by the signal form emitted by each D/A converter per datum or bit. By using a suitable signal form, such as – for example - multiple pulses, which consist of several pulses for each datum, the filter function can be improved selectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] These and other objects and advantages of the present invention will become more apparent and more readily appreciated from the following description of an exemplary embodiment, taken in conjunction with the accompanying drawings of which:

FIG 1 is a block diagram of a configuration for digital-analog conversion according to the invention, and

FIG 2, by way of comparison with FIG 1, is a block diagram of an exemplary embodiment of a configuration for digital-analog conversion according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout.

[0018] FIG 1 shows a block diagram of a configuration for digital-analog conversion according to the invention.

[0019] A high-frequency digital input signal DE arrives at a delay device VZ and at a converter device WD.

[0020] The delay device VZ has n delay elements VG1, VG2, VG3, ..., VGn, which are connected in a serially consecutive manner, and with a specific delay time τl, τ2, τ3, ..., τn being assigned to each of them. Each individual delay element VG1 to VGn is connected on the output side to an output VA1, VA2, VA3, ..., VAn of the delay device VZ. Via each of these

outputs VA1 to VAn, a delay signal VS1, VS2, VS3, ..., VSn, assigned thereto in each case and formed by the corresponding delay element VG1 to VGn, reaches an input WE1, WE2, WE3, ..., WEn on the conversion device WD.

[0021] The conversion device WD has a total of n+1 D/A converters W0, WI, ..., Wn, which are arranged in parallel to one another.
A first D/A converter W0 receives the digital input signal DE, as the input signal, via an input WE0 on the conversion device WD. The other n D/A converters receive the delay signals VS1 to VSn, as input signals, via correspondingly assigned inputs WE1 to WEn.

[0022] A specific coefficient k0, kl, ..., kn is assigned to each of the individual n+1 D/A converters WE0 to WEn of the conversion device WD.

[0023] The individual D/A converters W0 to Wn are combined on the output side, for example using n adding devices AE1, AE2, ..., AEn. Using the adding devices AE1 to AEn, n+1 output signals AS0, AS1,..., ASn of the n+1 D/A converters are added together to form a carrier-frequency analog output signal AA.

[0024] It should be noted that the digital input signals DE and VS1 to VSn are weighted, during the D/A conversion in the corresponding D/A converters W0 to Wn, with the respectively assigned coefficients k0 to kn.

[0025] These coefficients k0 to kn of the D/A converters W0 to Wn and the delay times $\tau 1$ to τn of the delay elements VG1 to VGn are defined such that a configuration for digital-analog conversion according to the invention has a required FIR filter characteristic.

[0026] FIG 2, by way of comparison with FIG 1, shows an exemplary embodiment of a configuration for digital-analog conversion according to the invention.

[0027] The individual D/A converters W0 to Wn are implemented as l-bit D/A converters and the delay elements VG1 to VGn as D latches. Both the D/A converters W0 to Wn and the delay elements VG1 to VGn are timed with a clock signal CLK.

[0028] The digital input signal DE is connected to the D input of a first D latch or of a first delay element VG1. On the output side, the first delay element VG1 is connected via its Q output to a D input of the next delay element VG2, etc.

[0029] Because of the clock signal CLK, the specific delay times τ1 to τn assigned to the individual delay elements VG1 to VGn correspond, as illustrated here, to half of a clock period of the clock signal CLK, which is likewise applied to the D/A converters W0 to Wn. Each individual delay element or D latch effects a delay of half of a clock period.

[0030] However, smaller sections of the clock period of the clock signal CLK may be used for the delay elements VG1 to VGn. This facilitates a more precise adjustment to an impulse response of a required filter characteristic. This in turn multiplies the Nyquist frequency of the filter characteristic and suppresses the alias effect.

[0031] The coefficients k0 to kn assigned to the individual D/A converters W0 to Wn are set with the help of reference current sources ki*Iref (in which i=0 to n), which determine the amplitude of the output signals AS0 to ASn.

[0032] If negative factors are required in the coefficients k0 to kn in order to realize the FIR filter characteristic, then corresponding outputs are exchanged in the D/A converters affected.

[0033] This is shown, by way of example, for the coefficients k2 and kn. The connections for the outputs are exchanged in the corresponding D/A converters W2 and Wn compared to the D/A converter WI (see detail D).

[0034] The output signals AS0 to ASn in the D/A converters W0 to Wn are added together at the same time and form the analog output signal AA.

[0035] The high-frequency digital input signal DE can also be in the form of a broadband signal in this invention.

[0036] The invention has been described in detail with particular reference to preferred embodiments thereof and examples, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention covered by the claims which may include the phrase "at least one of A, B and C" as an alternative expression that means one or more of A, B and C may be used, contrary to the holding in *Superguide v. DIRECTV*, 69 USPQ2d 1865 (Fed. Cir. 2004).